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**SEARCH REQUEST FORM** Scientific and Technical Information Center - EIC2800  
 Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 8/26/02 Serial # 16/022245 Priority Application Date 12/14/00  
 Your Name M. heois Examiner # \_\_\_\_\_  
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 In what format would you like your results? Paper is the default.  PAPER  DISK  EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB  
 Other: 08-26-02 P03:11 OUT

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements.

What types of references would you like? Please checkmark:

Primary Refs  Nonpatent Literature \_\_\_\_\_ Other \_\_\_\_\_  
 Secondary Refs  Foreign Patents \_\_\_\_\_  
 Teaching Refs \_\_\_\_\_

What is the topic, such as the novelty, motivation, utility, or other specific facets defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-26

Problem Page 2 lines Paragraph 7  
 " 3 " 8-10

Solution: " " " 11-13

Novelty in structure of claims.

Staff Use Only

Searcher: I. SPECKHARD  
 Searcher Phone: 308-6559

Searcher Location: STIC-EIC2800, CP4-9C18

Date Searcher Picked Up: 8/27/02

Date Completed: 8/28/02

Searcher Prep/Rev Time: 100

Online Time: 135

Type of Search

Structure (#) \_\_\_\_\_

Bibliographic  \_\_\_\_\_

Litigation \_\_\_\_\_

Fulltext  \_\_\_\_\_

Patent Family \_\_\_\_\_

Other \_\_\_\_\_

Vendors

STN  \_\_\_\_\_

Dialog  \_\_\_\_\_

Questel/Orbit \_\_\_\_\_

Lexis-Nexis \_\_\_\_\_

WWW/Internet \_\_\_\_\_

Other \_\_\_\_\_

08/28/2002 10/022,297

(FILE 'HOME' ENTERED AT 13:26:38 ON 28 AUG 2002)

FILE 'REGISTRY' ENTERED AT 13:28:23 ON 28 AUG 2002

L1 1 SEA ABB=ON PLU=ON ALUMINUM/CN  
L2 1 SEA ABB=ON PLU=ON ALUMINIUM/CN  
L3 1 SEA ABB=ON PLU=ON COPPER/CN  
L4 2 SEA ABB=ON PLU=ON (L1 OR L2 OR L3)

FILE 'HCAPLUS' ENTERED AT 13:30:28 ON 28 AUG 2002

L5 1306106 SEA ABB=ON PLU=ON ALUMINIUM OR ALUMINUM OR AL OR MOLTEN OR  
PYROPHORIC  
L6 266346 SEA ABB=ON PLU=ON (L1 OR L2)  
L7 1318543 SEA ABB=ON PLU=ON L5 OR L6  
L8 1010019 SEA ABB=ON PLU=ON COPPER OR CU OR L3  
L9 200164 SEA ABB=ON PLU=ON (LAND OR LAYER##### OR COAT##### OR  
FILM#####) AND L8  
L10 88123 SEA ABB=ON PLU=ON SUBSTRATE AND L7  
L11 158301 SEA ABB=ON PLU=ON SEMICONDUCT#####(1A) DEVICE  
L12 414584 SEA ABB=ON PLU=ON SEMICONDUCT#####  
L13 785234 SEA ABB=ON PLU=ON CHIP OR LEAD OR FRAME  
L14 38315 SEA ABB=ON PLU=ON RECTANG##### OR (RIGHT(3A)ANGLE##)  
L15 2622 SEA ABB=ON PLU=ON L13 AND L14  
L16 5155 SEA ABB=ON PLU=ON SOLDER#####(3A) (LAYER##### OR FILM##### OR  
COAT#####)  
L17 104881 SEA ABB=ON PLU=ON (SYNTHET##### OR ARTIFIV#####)(3A) (EPOX  
### OR RESIN OR THERMOPLASTIC##### OR ELASTOMER## OR RUBBER OR  
ADHESIVE##)  
L18 1076578 SEA ABB=ON PLU=ON EPOX### OR RESIN OR THERMOPLASTIC### OR  
ELASTOMER## OR RUBBER OR ADHESIVE##  
L19 52067 SEA ABB=ON PLU=ON POLYIMIDE OR POLYIMIDO  
L20 5353 SEA ABB=ON PLU=ON IMIDO OR IMIDE###(2A) POLYMER###  
L21 82659 SEA ABB=ON PLU=ON RESIN###(3A) (LAYER##### OR FILM##### OR  
COAT###)  
L22 10331 SEA ABB=ON PLU=ON L10 AND L9  
L23 158301 SEA ABB=ON PLU=ON L11 AND L12  
L24 1144 SEA ABB=ON PLU=ON L22 AND L23  
L25 1 SEA ABB=ON PLU=ON L24 AND L15  
D BIB AB 1  
L26 1143 SEA ABB=ON PLU=ON L24 NOT L25  
L27 25 SEA ABB=ON PLU=ON L26 AND L16  
L28 25 SEA ABB=ON PLU=ON L27 AND (L16 OR L17 OR L18 OR L19 OR L20  
OR L21 OR POLYMER OR HOMOPOLYMER OR COPOLYMER)  
L29 1 SEA ABB=ON PLU=ON L28 AND L17  
D BIB AB 1  
L30 24 SEA ABB=ON PLU=ON L28 NOT L29  
L31 24 DUP REM L30 (0 DUPLICATES REMOVED)  
D BIB AB 1-24  
L32 17091 SEA ABB=ON PLU=ON L23 AND (L16 OR L17 OR L18 OR L19 OR L20  
OR L21 OR POLYMER OR HOMOPOLYMER OR COPOLYMER)  
L33 25 SEA ABB=ON PLU=ON L32 AND L15  
L34 25 SEA ABB=ON PLU=ON L33 NOT L28  
L35 0 SEA ABB=ON PLU=ON L34 AND L10  
L36 0 SEA ABB=ON PLU=ON L34 AND L9

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L37 2 SEA ABB=ON PLU=ON L34 AND L7  
D BIB AB 1-2  
D HIS30-  
L38 23 SEA ABB=ON PLU=ON L34 NOT L37  
L39 0 SEA ABB=ON PLU=ON L38 AND L8  
L40 0 SEA ABB=ON PLU=ON L38 AND L16  
L41 0 SEA ABB=ON PLU=ON L38 AND (L16 OR L17)  
L42 23 DUP REM L38 (0 DUPLICATES REMOVED)  
D BIB AB 1-23  
L43 23 SEA L42  
L44 0 SEA ABB=ON PLU=ON L43 NOT L34  
L45 23 SEA L42  
L46 24 SEA L31  
L47 23 SEA ABB=ON PLU=ON L45 NOT L46

08/28/2002 10/022,297

L25 ANSWER 1 OF 1 HCPLUS COPYRIGHT 2002 ACS  
AN 2000:570164 HCPLUS  
DN 133:143451  
TI Ceramic **substrate** for preventing deformation caused by heat  
stress in power transistors  
IN Kwon, Heung-kyu  
PA Samsung Electronics Co., Ltd., S. Korea  
SO Repub. Korea, No pp. given  
CODEN: KRXXFC  
DT Patent  
LA Korean  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
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PI	KR 9710110	B1	19970621	KR 1994-19573	19940809

AB At the center of the ceramic base material made of **rectangular**  
Al2O3, at least one slot is formed. And 2 seats are formed on the base  
material to install **semiconductor devices** such as a  
power transistor. The wiring pattern and **semiconductor**  
**chip** are bonded to wire. At the bottom of the base material on  
which wiring pattern is formed, a heat sink thin **film** made of  
high conductive metal, such as Cu, Al, and Ag is  
formed for a better adhesion with heat sink. Therefore, by forming slot  
on the ceramic base material, deformation caused by heat stress or mech.  
reason can be prevented.

L29 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2002 ACS  
 AN 1967:468678 HCAPLUS  
 DN 67:68678  
 TI **Semiconductor devices**  
 PA Matsushita Electronics Corp.  
 SO Fr., 6 pp.  
 CODEN: FRXXAK  
 DT Patent  
 LA French  
 FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	FR 1457006		19661028		
PRAI	JP		19641026		

AB Two or more electrodes of a **semiconductor device** are connected to the leads of a tight capsule by using a transparent and insulating **substrate** on which a metallic thin **film** is deposited. The metallic thin-film pattern is so designed that its extreme points correspond to the **semiconductor** electrodes. At first the back face of the **semiconductor** is soldered to the metallic socket of the capsule, then the transparent and insulating **substrate** is superposed on the **semiconductor**, the 2 surfaces are bonded together, and the leads of the capsule are soldered to the thin **film** deposited on the transparent **substrate**. The capsule is made tight by applying a **synthetic resin** or a low-melting glass. As the **semiconductor**, a transistor of the planar or mesa type is used. This **semiconductor** can be also of an integrated-circuit type. Another possibility is to use a band of evenly spaced **semiconductors** on which an insulating **substrate** band with deposited thin-film patterns is superposed and bonded. Then, the band is cut into small pieces which each represent an independent **semiconductor** circuit, and these are connected sep. to the tight capsules. The transistor is soldered to its socket with a Au alloy. On the glass of quartz **substrates**, the metallic thin **film** (of Pt, In, Au, Cu, Al, Ag, or certain of their alloys) is deposited by a vacuum procedure with the use of the masking technique. The whole system is soldered to the transistor by thermocompression bonding in an inert gas atm. Before bonding, the extreme points of the metallic thin **film** are superposed, precisely, on the transistor electrodes by controlling their position under a microscope, which is facilitated by the **substrate** transparency. The lateral sides of the **substrate** are provided with 2 semicircular notches anticipated for the passage of capsule leads. The leads are fixed to the thin **film** by applying a soft solder. In such a way, it is possible to avoid the earlier encountered difficulties when working with classic wire-lead connections.

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L31 ANSWER 1 OF 24 HCAPLUS COPYRIGHT 2002 ACS  
AN 2002:392083 HCAPLUS  
DN 136:394356

TI Method of forming solder bumps on integrated circuit **substrate**

IN Hu, Chu-Chin

PA Taiwan

SO U.S. Pat. Appl. Publ., 8 pp.

CODEN: USXXCO

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002060160	A1	20020523	US 2001-796268	20010228
PRAI	TW 2000-89117431	A	20000829		

AB The method first deposits a medium **layer** on a protective **layer** of the integrated circuit (IC) package **substrate**, which has good adherence ability to both the **Cu layer** and the protective **layer**. A CVD process is applied to deposit a **Cu layer** on the medium **layer** to form the metal **layer**. A dry **film** is formed on the metal **layer** and several contact windows are opened. A metal pad and a bump are electroplated in the contact windows. Then remove the dry **film**, the bumps are protruded out of the **substrate** with a predetd. height to be solder bumps with an IC chip. By said method, an IC chip no longer needs to form bumps thereon anymore and saves cost and reduces pitch between bumps down to 150 .mu.m. Package size is scaled for smaller IC chips and for smaller component dimension.

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L31 ANSWER 2 OF 24 HCPLUS COPYRIGHT 2002 ACS  
AN 2002:327890 HCPLUS  
DN 136:333907  
TI Method of fabricating **semiconductor** package having metal peg  
leads and connected by trace lines  
IN Liu, Wen-Chun  
PA Walsin Advanced Electronics Ltd., Taiwan  
SO U.S., 13 pp.  
CODEN: USXXAM  
DT Patent  
LA English  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6380062	B1	20020430	US 2001-802796	20010309

AB The present invention relates to a method of manufg. **semiconductor** ball grid array package with metal peg leads, all connected by trace lines. The ball grid array package has internal trace lines and exposed metal pegs. A metal **substrate** is provided. Electroplated **layers** are formed over metal peg regions and a die pad region on the surface of the metal **substrate**. A **layer** of **substrate** material at the top surface of the metal **substrate** is removed so that thickness of the metal **substrate** is reduced. Hence, trace lines, die pad and internal metal pegs are formed. A die is attached to the die pad and elec. connections from the die to the internal metal pegs are made. A molding process is carried out to enclose the die, the die pad and the internal metal pegs on 1 side of the metal **substrate** with plastic material. The lower surface of the metal **substrate** is etched to form external metal pegs while exposing the mold material and the bottom surface of the die pad. The internal metal pegs and the external metal pegs are interconnected via the trace lines. A **soldering** mask **layer** is formed over the package surface covering the trace lines but exposing the electroplated at the end face of each external metal peg.

RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD  
ALL CITATIONS AVAILABLE IN THE RE FORMAT

08/28/2002 10/022,297

L31 ANSWER 3 OF 24 HCPLUS COPYRIGHT 2002 ACS  
AN 2002:592468 HCPLUS  
TI Power modules, composite **substrates** for modules thereof, and  
brazes applied to composite formation thereof  
IN Suzuki, Kiyomitsu; Abe, Teruyoshi; Kondo, Yasuo; Watabe, Noriyuki;  
Suzumura, Takashi; Nakagawa, Kazuhiko  
PA Hitachi Ltd., Japan; Hitachi Cable, Ltd.  
SO Jpn. Kokai Tokkyo Koho, 6 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
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PI JP 2002222905 A2 20020809 JP 2001-16821 20010125

AB The title power modules comprise a ceramic **substrate** provided  
with a circuit **layer** on the front surface and a heat-releasing  
plate on the rear surface, a heat sink **substrate** bound to the  
heat-releasing plate with a 1st metallic braze, and a  
**semiconductor** power component bound to the circuit **layer**  
with a 2nd metallic braze. The one of the 1st and 2nd brazes is a  
Ag-alloy (m.p. 500-600.degree.) chosen from Ag-Cu-Sn, Ag-  
Cu-In, or Ag-Cu-Sn-In and the other is a solder. The  
use of the braze combination gives the formation of the modules minimized  
binding strain and reliable binding.

08/28/2002 10/022,297

L31 ANSWER 4 OF 24 HCPLUS COPYRIGHT 2002 ACS  
AN 2002:486560 HCPLUS  
DN 137:40364  
TI Power **semiconductor devices**  
IN Morita, Koji; Murai, Takayuki; Yoshikawa, Takao  
PA Yamaha Motor Co., Ltd., Japan  
SO Jpn. Kokai Tokkyo Koho, 3 pp.  
CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2002184907	A2	20020628	JP 2000-379569	20001214
AB	The title devices have a <b>semiconductor</b> chip mounted and packaged on an Al <b>substrate</b> pad and sealed with a <b>polymer</b> , wherein the devices are connected via a <b>solder layer</b> on the Cu pad. The arrangement gives the devices simplified and increased chip packaging.				

08/28/2002 10/022,297

L31 ANSWER 5 OF 24 HCPLUS COPYRIGHT 2002 ACS  
AN 2002:273331 HCPLUS  
DN 136:317783  
TI Ceramic circuit boards comprising ceramic insulating **substrates** and metal sheets for **semiconductor devices**  
IN Sasaki, Yasuhiro; Terao, Shinya  
PA Kyocera Corp., Japan  
SO Jpn. Kokai Tokkyo Koho, 5 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE	
-----	-----	-----	-----	-----	-----	
PI	JP 2002111211	A2	20020412	JP 2000-296940	20000928	
AB	Ceramic circuit boards are manufd. by joining <b>Al-</b> or <b>Cu</b> -based metal sheets to ceramic insulating <b>substrates</b> through a <b>solder</b> joining <b>layer</b> to form wiring <b>layer</b> (s) or heat sink, wherein the centerline av. roughness (Ra) of the joining surface between the ceramic insulating <b>substrates</b> and the metal sheets is 0.05-10 .mu.m and a 1-10 .mu.m thick metal <b>layer</b> having excellent wettability with the solder is formed on the ceramic circuit boards. The ceramic insulating <b>substrates</b> are made from Al2O3, AlN, and/or Si3N4, and the metal <b>layer</b> is formed from <b>Al</b> , <b>Ni</b> , or <b>Cu</b> .					

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

08/28/2002 10/022,297

L31 ANSWER 6 OF 24 HCPLUS COPYRIGHT 2002 ACS  
AN 2002:193572 HCPLUS  
DN 136:240083  
TI Insulative ceramic **substrates**, manufacturing, and power-  
semiconductor multilayer circuit boards using **substrates**  
thereof  
IN Ishiwatari, Hiroshi; Tanaka, Akira; Taniguchi, Yasuhiko; Shimizu, Toshio;  
Hiramoto, Hiroyuki; Komorita, Hiroshi; Nanami, Takayuki  
PA Toshiba Corp., Japan  
SO Jpn. Kokai Tokkyo Koho, 13 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
	-----	-----	-----	-----	-----
PI	JP 2002076214	A2	20020315	JP 2000-257084	20000828
AB	The title circuit boards comprise a multilayer of ceramic <b>substrates</b> which are provided on their both sides with a conductive <b>layer</b> and laminated by <b>soldering</b> , brazing, binding with an active metal <b>layer</b> , or adhering with thermal-conductive org. <b>polymers</b> . The insulative ceramic <b>substrates</b> may be made of AlN or Al2O3 in economical process. The ceramic multilayer circuit boards gives the power <b>semiconductor devices</b> improved insulative withstand voltage horizontally as well as perpendicularly to the lamination against high current and voltage.				

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L31 ANSWER 7 OF 24 HCPLUS COPYRIGHT 2002 ACS  
AN 2002:301197 HCPLUS  
DN 137:101334  
TI Fabrication of a cylindrical display by patterned assembly  
AU Jacobs, Heiko O.; Tao, Andrea R.; Schwartz, Alexander; Gracias, David H.;  
Whitesides, George M.  
CS Department of Electrical Engineering, University of Minnesota,  
Minneapolis, MN, 55455, USA  
SO Science (Washington, DC, United States) (2002), 296(5566), 323-325  
CODEN: SCIEAS; ISSN: 0036-8075  
PB American Association for the Advancement of Science  
DT Journal  
LA English  
AB The authors demonstrate fabrication of the patterned assembly of  
integrated **semiconductor devices** onto planar,  
flexible, and curved **substrates** based on capillary interactions  
involving liq. solder. The **substrates** presented patterned,  
**solder-coated** areas that acted both as receptors for the  
components of the device during its assembly and as elec. connections  
during its operation. The components were suspended in water and agitated  
gently. Minimization of the free energy of the solder-water interface  
provided the driving force for the assembly. One hundred and thirteen  
GaAlAs light-emitting diodes with a chip size of 280 .mu.m were fabricated  
into a prototype cylindrical display. It was also possible to assemble  
1500 silicon cubes, on an area of 5 square centimeters, in less than 3  
min, with a defect rate of .apprx.2%. Addnl. information of the  
fabrication of the receptor arrays, the LED's, and the Si blocks, as well  
as the procedures to control the surface chem. are provided at  
[www.sciencemag.org/cgi/content/full/296/5566/323/DC1](http://www.sciencemag.org/cgi/content/full/296/5566/323/DC1).  
RE.CNT 26 THERE ARE 26 CITED REFERENCES AVAILABLE FOR THIS RECORD  
ALL CITATIONS AVAILABLE IN THE RE FORMAT

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L31 ANSWER 8 OF 24 HCPLUS COPYRIGHT 2002 ACS  
AN 2001:611707 HCPLUS

DN 135:161252

TI Inexpensive and reliable BGA package for high density cavity-up wire bond device connections using a metal panel, thin **film** and build up multilayer technology

IN Ho, Chung Wen

PA Thin Film Module, Inc., Taiwan

SO U.S., 11 pp.

CODEN: USXXAM

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6277672	B1	20010821	US 1999-389634	19990903
	US 2001046725	A1	20011129	US 2001-900558	20010709
PRAI	US 1999-389634	XX	19990903		

AB A new method is provided for mounting high-d. wire bond **semiconductor devices**. A **layer** of dielec. is deposited over the 1st surface of a metal panel. One or more thin **film** interconnect **layers** are then created on top of the dielec. **layer**. The BUM technol. allows for the creation of a succession of **layers** over the thin **film** **layers**

. The combined **layers** of thin **film** and BUM form the interconnect **substrate**. One or more cavities are created in the 2nd surface of the metal panel; openings through the **layer** of dielec. are created where the **layer** of dielec. is exposed. One or more wire bond **semiconductor** die are inserted into the cavities, are die bonded and wire bonded to the openings that were created in the **layer** of dielec. Openings are created in the bottom BUM **layer**; solder balls are inserted and attached to this BUM **layer** for the completion of the Ball Grid Array (BGA) package.

RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD  
ALL CITATIONS AVAILABLE IN THE RE FORMAT

08/28/2002 10/022,297

L31 ANSWER 9 OF 24 HCPLUS COPYRIGHT 2002 ACS  
AN 2001:747340 HCPLUS  
DN 135:292447  
TI Lead-free solder joints for **semiconductor devices**  
IN Tadauchi, Masahiro; Matsuo, Mie; Nakamura, Shinichi; Komatsu, Izuru;  
Tejima, Koichi  
PA Toshiba Corp., Japan  
SO Jpn. Kokai Tokkyo Koho, 6 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001284384	A2	20011012	JP 2000-96447	20000331

AB The joint comprises (a) a **semiconductor substrate**, (b) a conductive metal **layer**, (c) an alloy **layer** of Zn or Ag with the metal in **layer b**, (d) a Sn-rich **layer**, and (e) a Pb-free **solder layer** mainly consisting of Sn and contg. the said metals. Diffusion of the solder materials into the **semiconductor substrates** is prevented.

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08/28/2002 10/022,297

L31 ANSWER 10 OF 24 HCPLUS COPYRIGHT 2002 ACS  
AN 2001:617459 HCPLUS  
DN 135:187509  
TI Group III **semiconductor** laser **devices**  
IN Nagai, Seiji; Ito, Suguru; Yuguchi, Mitsuo; Koike, Masayoshi  
PA Toyota Gosei Co., Ltd., Japan  
SO Jpn. Kokai Tokkyo Koho, 13 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001230498	A2	20010824	JP 2000-38279	20000216

AB The devices comprise: a **Cu** heat sink; a Sn/In **solder** **layer**; a nickel **layer**; a pair of Au/Mo electrodes bonding a Au/Mo/Rh anode and a Ni cathode; and a p-AlGaAs cladding, an active, an n-AlGaAs cladding, an AlN buffer and a sapphire **substrate**.

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L31 ANSWER 11 OF 24 HCAPLUS COPYRIGHT 2002 ACS  
AN 2001:29155 HCAPLUS  
DN 134:94313  
TI Fabrication of wafer chip-size-package **semiconductor**  
**devices**  
IN Miyata, Masahiro; Ezawa, Hirokazu  
PA Toshiba Corp., Japan  
SO Jpn. Kokai Tokkyo Koho, 6 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001007135	A2	20010112	JP 1999-176312	19990623

AB The title fabrication wafer chip-size-package (CSP) **semiconductor**  
**devices** involves forming a bump electrode over a barrier metal  
film and an contact pad on a **semiconductor**  
**substrate**, **coating** an org. **polymer**  
**film** to cover the bump electrode over the entire **substrate**  
, etching back the **substrate** surface to expose the bump  
electrode, curing the org. **polymer film**, and forming a  
**solder** ball on the bump electrode. The bump electrode may be made  
of Cu, Ni, or Au which gives a good wettability to the solder  
ball formation.

08/28/2002 10/022,297

L31 ANSWER 12 OF 24 HCPLUS COPYRIGHT 2002 ACS  
AN 2000:636235 HCPLUS  
DN 133:216532  
TI Fabrication of **semiconductor** component with external contact  
polymer support  
IN Farnsworth, Warren M.; Wood, Alan G.  
PA Micron Technology, Inc., USA  
SO U.S., 13 pp.  
CODEN: USXXAM  
DT Patent  
LA English  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6118179	A	20000912	US 1999-384783	19990827
	US 6180504	B1	20010130	US 1999-440380	19991115
PRAI	US 1999-384783	A3	19990827		

AB A **semiconductor** component includes a **substrate**, bonding pads on the **substrate**, and external contacts bonded to the bonding pads. Exemplary external contacts include solder balls, solder bumps, solder columns, TAB bumps and stud bumps. Preferably the external contacts are arranged in a dense array, such as a ball grid array (BGA), or fine ball grid array (FBGA). The component also includes a polymer support member configured to strengthen the external contacts, absorb forces applied to the external contacts, and prevent sepn. of the external contacts from the bonding pads. In a first embodiment, the polymer support member comprises a cured polymer layer on the **substrate**, which encompasses the base portions of the external contacts. In a second embodiment, the polymer support member comprises support rings which encompass the base portions of the external contacts. In either embodiment the polymer support member transfers forces applied to the external contacts away from the interface with the bonding pads, and into the center of the contacts.

RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD  
ALL CITATIONS AVAILABLE IN THE RE FORMAT

08/28/2002 10/022,297

L31 ANSWER 13 OF 24 HCPLUS COPYRIGHT 2002 ACS  
AN 2000:197893 HCPLUS

DN 132:211606

TI **Copper** sheet-joined nitride ceramic **substrates** having  
high reliability for **semiconductor devices**

IN Uchida, Shinji

PA Fuji Electric Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 7 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000086368	A2	20000328	JP 1998-261177	19980916

AB A braze **layer** from **Cu**, **Ag**, or **Cu-Ag** type  
alloys contg. active metals is formed on nitride ceramic  
**substrates**, and the braze **layer** is joined with  
**Cu** sheets by soldering to obtain nitride ceramic  
**substrates** for **semiconductor devices**. The  
nitride ceramic plates are **AlN** or **Si3N4** sintered plates.

08/28/2002 10/022,297

L31 ANSWER 14 OF 24 HCPLUS COPYRIGHT 2002 ACS  
AN 1999:719059 HCPLUS  
DN 131:331076  
TI Cast metal seal for **semiconductor substrates**  
IN Toy, Hilton T.; Bolde, Lannie R.; Covell, James H., II; Edwards, David L.;  
Goldmann, Lewis S.; Gruber, Peter A.  
PA International Business Machines Corporation, USA  
SO U.S., 10 pp.  
CODEN: USXXAM

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
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PI US 5982038 A 19991109 US 1997-850092 19970501

AB The invention relates generally to a new scheme of providing a seal for **semiconductor substrates** and chip carriers. More particularly, the invention encompasses a structure and a method that uses a multilayer metallic seal to provide protection to chips on a chip carrier. This multilayer metal seal provides both enhanced hermeticity lifetime and environmental protection. For the preferred embodiment, the multilayer metallic seal is a **2-layer solder** structure which is used to create a low-cost, high-reliability, hermetic seal for the module. This solder structure has a thick high-m.p. region that is attached to a cap, and a thin interconnecting region of lower m.p. for sealing the **substrate** to the cap.

RE.CNT 24 THERE ARE 24 CITED REFERENCES AVAILABLE FOR THIS RECORD  
ALL CITATIONS AVAILABLE IN THE RE FORMAT

08/28/2002 10/022,297

L31 ANSWER 15 OF 24 HCPLUS COPYRIGHT 2002 ACS  
AN 1999:610940 HCPLUS  
DN 131:236653  
TI **Copper-beryllium alloy lead for semiconductor**  
device showing high resistance to peeling from solder under  
heating  
IN Uno, Takao  
PA Furukawa Electric Co., Ltd., Japan  
SO Jpn. Kokai Tokkyo Koho, 5 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11260993	A2	19990924	JP 1998-61126	19980312
AB	The lead is made of a Cu alloy contg. 0.2-3.0 wt.% of Be and having a Zn <b>layer</b> or a Cu-Zn alloy <b>layer</b> (contg. .gtoreq.10 wt.% of Zn) at a part to be soldered. The Cu alloy may further contain 0.001-5.0 wt.% (as total) of Ni, Co, Fe, Si, Pb, Al, Zr, Mg, Ag, and/or Te in addn. to Be. By arranging the Zn <b>layer</b> or the Cu-Zn alloy <b>layer</b> , adhesion strength of the Cu-Be alloy to Pb solder is improved.				

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

L31 ANSWER 16 OF 24 HCPLUS COPYRIGHT 2002 ACS  
AN 2000:651912 HCPLUS  
DN 133:328110  
TI 3D Si-on-Si stack package  
AU Kanbach, H.; Wilde, J.; Kriebel, F.; Meusel, E.  
CS DaimlerChrysler AG, Research & Technology, Lab Microelectronics,  
Frankfurt/Main, D-60528, Germany  
SO Proceedings of SPIE-The International Society for Optical Engineering  
(1999), 3830(International Conference on High Density Packaging and MCMs,  
1999), 248-253  
CODEN: PSISDG; ISSN: 0277-786X  
PB IMAPS - International Microelectronics and Packaging Society  
DT Journal  
LA English  
AB Future electronic systems have to satisfy an increasing demand in respect  
of: Small vol., lightwt., operation at high frequencies and speed, high  
power levels, sensitive and smart functions and cost effectiveness. An  
attractive approach for meeting these requirements is the 3-dimensional  
(3D) electronic packaging. Starting from the state of the art this paper  
presents a new concept of 3D-electronic packaging. The approach can be  
described as a Si-on-Si multi chip module flip chip technol. with arrays  
of fine etched and filled vertical elec. interconnections (vias). In  
contrast to existing concepts our concept uses area arrays of vias with a  
high no. of interconnections and not only peripheral interconnections. A  
3D Si-on-Si stack package demonstrator has been realized. The  
demonstrator (12.5 .times. 12.5 .times. 2.3 mm<sup>3</sup>) consists of 4 Si-  
**substrates** each representing a system level and contg. 4 thinned  
and as flip chip assembled chips. In the outer part of the Si-  
**substrates** there are 3 rows of vertical interconnections each with  
a diam. of 110 .mu.m and a length of 500 .mu.m. The vias are isolated,  
metalized and **coated** with WTi/Cu/Au. The chips are  
flip chip mounted in the flat side of the Si-**substrates** on  
appropriate pads and metal **layers**. When interconnecting the Si-  
**substrates** to each other by bump technol. the chips submerge into  
cavities on the rear side of the adjacent Si-**substrate**.  
Altogether there are 12 chips integrated in the 3D-stack package  
demonstrator. The chips also test the technol. and quality of the  
electronic packaging. For this purpose they contain a set of thin  
film heaters, junctions for temp. measuring, Al-meanders  
for stress and strain measuring and daisy chains for conduction paths  
controlling. Key technologies are anisotropic reactive ion etching,  
metalization, filling of the vias and the flip chip technol. with solder  
or **polymer** bumps.

RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD  
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31 ANSWER 17 OF 24 HCPLUS COPYRIGHT 2002 ACS  
 AN 1998:398503 HCPLUS  
 DN 129:75005  
 TI Electronic component and **semiconductor device**, method  
 for manufacturing and mounting thereof, and circuit board and electronic  
 equipment  
 IN Hashimoto, Nobuaki  
 PA Seiko Epson Corporation, Japan; Hashimoto, Nobuaki  
 SO PCT Int. Appl., 73 pp.  
 CODEN: PIXXD2  
 DT Patent  
 LA Japanese  
 FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE	
PI	WO 9825297	A1	19980611	WO 1997-JP4437	19971204	
	W: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HU, ID, IL, IS, JP, KE, KG, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM RW: GH, KE, LS, MW, SD, SZ, UG, ZW, AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG					
	CN 1206494	A	19990127	CN 1997-191450	19971008	
	AU 9851363	A1	19980629	AU 1998-51363	19971204	
	CN 1210621	A	19990310	CN 1997-192032	19971204	
PRAI	JP 1996-339045	A	19961204			
	JP 1996-356880	A	19961226			
	JP 1997-91449	A	19970326			
	WO 1997-JP4437	W	19971204			
AB	A <b>semiconductor device</b> whose package size is nearly the same as the size of a chip, which has a stress absorbing <b>layer</b> , which does not require a flexible <b>substrate</b> , and which can be manufd. in a large no. at the same time. A method for manufg. a <b>semiconductor device</b> includes a process wherein electrodes are formed on a wafer, a process wherein a <b>resin</b> <b>layer</b> is formed as a stress reducing <b>layer</b> on the wafer except for the parts where the electrodes are formed, a process wherein a Cr <b>layer</b> is formed as an interconnect on the whole surface of the wafer including the electrodes and the <b>resin layer</b> , a process wherein <b>solder</b> balls are formed as external electrodes on parts of the chrome <b>layer</b> which are formed on the <b>resin layer</b> , and a process wherein the wafer is diced to <b>semiconductor</b> chips. In the processes for forming the chrome <b>layer</b> and for forming the solder balls, a metal thin <b>film</b> deposition technol. used in the wafer process of <b>semiconductor</b> manufg. is employed.					

08/28/2002 10/022,297

L31 ANSWER 18 OF 24 HCPLUS COPYRIGHT 2002 ACS  
AN 1997:341032 HCPLUS  
DN 127:27514  
TI Manufacture of **semiconductor device** having solder bump  
electrode  
IN Kanda, Koji  
PA Sanyo Electric Co., Ltd., Japan  
SO Jpn. Kokai Tokkyo Koho, 4 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
	-----	-----	-----	-----	-----
PI	JP 09097792	A2	19970408	JP 1995-251449	19950928

AB The title method involves the following steps; (A) opening an elec. insulating **film** to reach a metal pad on a **semiconductor substrate**, (B) forming an **Al**-plated electrode **film**, (C) forming a barrier metal **film** on the electrode **film**, (D) forming a photoresist **film**, (E) plating to form a solder bump electrode on the metal pad, (F) removing the photoresist **film**, (G) treating the plated electrode **film** with an alkali developer, and (H) reflowing the bump electrode. The electrode with good stable elec. characteristics and dimensional stability was obtained.

08/28/2002 10/022,297

L31 ANSWER 19 OF 24 HCPLUS COPYRIGHT 2002 ACS

AN 1996:508827 HCPLUS

DN 125:156246

TI Manufacture of bump electrode

IN Wakabayashi, Takeshi; Abe, Akihiko

PA Casio Computer Co Ltd, Japan

SO Jpn. Kokai Tokkyo Koho, 5 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE	
	-----	-----	-----	-----	-----	
PI	JP 08172096	A2	19960702	JP 1994-334322	19941216	
AB	The title method involves the following steps; forming a protective film on a <b>substrate</b> , forming a <b>layer</b> for formation of a metal underlayer on the protective <b>film</b> and a contact pad in a hole of the protective <b>film</b> , forming a 50-150-.mu.m plating resist <b>layer</b> , and forming a <b>solder</b> columnar bump electrode in the hole. A bump electrode with enough height was obtained.					

08/28/2002 10/022,297

L31 ANSWER 20 OF 24 HCPLUS COPYRIGHT 2002 ACS  
AN 1994:225049 HCPLUS  
DN 120:225049  
TI Sintered aluminum nitride **substrate** having metalized  
layers  
IN Ogata, Yasunobu; Yoshizoe, Sumio  
PA Hitachi Metals Ltd, Japan  
SO Jpn. Kokai Tokkyo Koho, 3 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06032687	A2	19940208	JP 1992-190363	19920717

AB The AlN **substrate** has multiple metalized **layers** and a  
**solder layer** as the outmost **layer**. The  
formation of multiple metalized **layers** improves **solder**  
wettability and solder adhesion.

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

L37 ANSWER 2 OF 2 HCPLUS COPYRIGHT 2002 ACS  
AN 1967:495180 HCPLUS  
DN 67:95180  
TI Encapsulated multi-terminal **semiconductor** devie  
IN Hill, John  
PA International Standard Electric Corp.  
SO U.S., 5 pp.  
CODEN: USXXAM  
DT Patent  
LA English  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
	-----	-----	-----	-----	-----
PI	US 3324357		19670606		
PRAI	GB		19640129		

AB A method is described for providing an encapsulated **semiconductor** **device** which includes a wafer having opposite cond. type electrodes, a header for mounting the wafer including **lead** wires, and solder contacts between electrodes and **lead** wires. Preformed n-p-n transistors formed in a slice of n-type Si with a layer of Si oxide as a diffusion mask are used as an example. **Al** contacts to the collector, base, and emitter regions are formed by known techniques. Au-Cr metallic film, large area contacts are formed over the **Al** contacts. The slice is dipped in a fluxing soln. and then in a solder bath which forms low mounds of solder on the contacts. The slice is sepd. into wafers for mounting. The header has 3 **lead** wires passing through a glass-metal seal and projecting on the other side. The **lead** wires are formed by bending these ends inward toward each other, and a flat is produced on each end. The flats are approx. coplanar and at **right angles** to the direction of the **leads** on the far side of the seal. The mounting is conducted so that the solder on each of the contacts of the wafer is in contact with the appropriate **lead** wire flat. The assembly is heated by radiation or other suitable means. The solder melts and wets the **lead** wire ends. After cooling, the assembly is washed and dried to remove any contaminants. Final encapsulation is effected by fixing a metal cap over the header by resistance "projection" welding. Alternatively, the wafer may be surrounded with a thermosetting **resin** which also fills the area between the wafer and the face of the header.

L42 ANSWER 1 OF 23 HCPLUS COPYRIGHT 2002 ACS  
AN 2002:573704 HCPLUS

DN 137:133195

TI **Semiconductor chip**-mounting packages and fabrication  
of packages thereof

IN Omura, Kenichi

PA Kyocera Corp., Japan

SO Jpn. Kokai Tokkyo Koho, 9 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
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PI JP 2002217327 A2 20020802 JP 2001-8916 20010117

AB The title packages comprise an insulator plate having a large **rectangular** through-hole in its central region for mounting a **semiconductor chip**, a pl. no. of circuit conductors provided on the upper surface of the insulator plate, ground and power circuit conductors provided on the lower surface of the insulator plate, a thermosetting **polymer** insulator layer covering over the ground and power circuit conductors, and a heat-releasing plate adhered to the insulator plate via the **polymer** insulator layer. The **polymer** insulator layer is recessed by 0.05-2 mm from its large **rectangular** through-hole edges so that the circuit conductors and the **chip** electrodes are secured for connection without excess insulator.

08/28/2002 10/022,297

L42 ANSWER 2 OF 23 HCPLUS COPYRIGHT 2002 ACS  
AN 2002:566153 HCPLUS  
DN 137:118035  
TI Screen printing masks and method for mounting **semiconductor**  
parts on circuit substrates using them  
IN Ikari, Takashi; Hirano, Masato; Yamaguchi, Atsushi  
PA Matsushita Electric Industrial Co., Ltd., Japan  
SO Jpn. Kokai Tokkyo Koho, 6 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE	
	-----	-----	-----	-----	-----	
PI	JP 2002211154	A2	20020731	JP 2001-15742	20010124	
AB	The mask, useful for supplying an <b>adhesive</b> material to substrate lands or electrode pads with a narrow pitch on <b>semiconductor</b> parts, has a plurality of through holes including those having oval and/or <b>rectangular</b> cross sections perpendicular to the thickness direction, wherein shapes of the lands or electrode pads may be identical to the cross sections. The method is esp. useful for fabricating BGA (ball grid array) and/or CSP ( <b>chip</b> size package).					

L42 ANSWER 3 OF 23 HCPLUS COPYRIGHT 2002 ACS

AN 2002:349916 HCPLUS

TI **Semiconductor device** and its production method.  
[Machine Translation].

IN Kasuya, Yasumasa

PA Rohm Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 7 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
	-----	-----	-----	-----	-----
PI	JP 2002134677	A2	20020510	JP 2000-322207	20001023
	US 2002096790	A1	20020725	US 2001-27856	20011019
PRAI	JP 2000-322207	A	20001023		

AB [Machine Translation of Descriptors]. Preventing the exfoliation of the **resin** package by the moisture which invades, it offers the **semiconductor device** whose reliability is high.

**Semiconductor chip 1** and this **semiconductor**

**chip 1** only loading through 1st wire 11, in island through the 2nd wire 12 of the plural books 2 of the plane surface apparent abbreviation **rectangular** condition which is connected to **semiconductor chip 1** electrically and **semiconductor chip 1**

it has with the plural inner **leads/reads** 3 which each one electrically are connected, **semiconductor chip 1** being the **semiconductor device S** which the **resin**

package is done when the underside of island 2 is exposed with the packaging **resin**, in the marginal vicinity of island 2, the underside 2b side cuts and is lacked and from the other part makes thin in thickness direction thin 5 It is formed, the slit 9 which is penetrated to the thickness direction is formed to thin 5.

L42 ANSWER 4 OF 23 HCAPLUS COPYRIGHT 2002 ACS  
AN 2002:349910 HCAPLUS  
TI **Semiconductor device** and its production method.  
[Machine Translation].  
IN Fujimoto, Hiroaki; Sahara, Ryuichi; Minamio, Masaki; Fukuda,  
Toshiyuki; Nomura, Toru  
PA Matsushita Electric Industrial Co., Ltd., Japan  
SO Jpn. Kokai Tokkyo Koho, 16 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2002134661	A2	20020510	JP 2000-326602	20001026

AB [Machine Translation of Descriptors]. That light weight conversion had become problem in accordance with the demand of small size light weight conversion of the electronic equipment, regarding the **semiconductor device** of BGA type. It possesses wiring electrode 1 in the surface, the wiring baseplate the **semiconductor chip** 4 where is loaded onto the surface of 3 which possesses ball electrode 2 in the base and wiring baseplate 3 and **semiconductor chip** the metal thin line from the insulated seal **resin** 6 where seals the surface of 5 which connects with the wiring electrode 1 of 4 and wiring baseplate 3 and wiring baseplate 3 it is constituted, the surface periphery of seal **resin** 6 seal **resin** 6 being deleted, has had hypotenuse section 10, when cubic measure of seal **resin** 6 of abbreviation **rectangular** parallelepiped form of imagination is designated as 100 % ], inside that 20 % ] The seal **resin** above is deleted. Because of this the seal **resin** quantity of the surface periphery is reduced substantially, weight is made to decrease, the **semiconductor device** of lightweight BGA type is actualized as a whole.

L42 ANSWER 5 OF 23 HCPLUS COPYRIGHT 2002 ACS  
AN 2002:273582 HCPLUS  
TI Resin seal type **semiconductor device** and its  
production method. [Machine Translation].  
IN Aoyama, Tomoyuki  
PA Matsushita Electric Industrial Co., Ltd., Japan  
SO Jpn. Kokai Tokkyo Koho, 7 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2002110728	A2	20020412	JP 2000-304569	20001004

AB [Machine Translation of Descriptors]. Until recently in as for the **semiconductor device** to be **rectangular** condition, to become large, the **lead/read frame** itself which is loaded large as a plane surface form, as for the small-sized **resin seal type semiconductor device** there was a theme that call by result it cannot be actualized. In spherical **semiconductor device** the point opposing 10 and that **semiconductor device** 10, the plural inner **lead** /read sections 4 which are arranged and each inner **lead**/read section the metal thin line 8 which connects with the electrode 11 of the surface of 4 and **semiconductor device** 10 and **semiconductor device** 10, inner **lead**/read section 4, the seal **resin** to connect 12 which seals the outside surrounding territory in metal thin line 8 and inner **lead**/read section 4, to be constituted from the outer **lead**/read section 5 which is exposed from seal **resin** 12, because spherical **semiconductor device** 10 is used, to hold down the enlargement of plane surface form, more small-sized **resin seal type semiconductor device** It can actualize.

08/28/2002 10/022,297

L42 ANSWER 6 OF 23 HCPLUS COPYRIGHT 2002 ACS

AN 2001:314144 HCPLUS

TI **Semiconductor device**

IN Horie, Yoshitaka; Maeda, Masahide

PA Rohm Co., Ltd., Japan

SO PCT Int. Appl.

CODEN: PIXXD2

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2001031704	A1	20010503	WO 2000-JP6858	20001002
	W: CN, KR, US				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	JP 2001196518	A2	20010719	JP 2000-126742	20000427
	TW 459279	B	20011011	TW 2000-89120630	20001004
PRAI	JP 1999-306341	A	19991028		
	JP 2000-126742	A	20000427		
AB	A <b>semiconductor device</b> (S1) comprising a <b>semiconductor chip</b> (5), a <b>chip</b> mounting <b>internal lead</b> (1) for mounting the <b>semiconductor chip</b> (5), <b>chip</b> connecting <b>internal leads</b> (2, 3) electrically connected to the upper surface of the <b>semiconductor chip</b> (5), and a <b>resin package</b> (7), <b>rectangular</b> as seen in a plan view, enclosing the <b>semiconductor chip</b> (5) and <b>internal leads</b> (1-3). The end of the <b>chip</b> mounting <b>internal lead</b> (1) is a <b>rectangle</b> or substantially <b>rectangle</b> extending longitudinally of the <b>resin package</b> (7).				
RE.CNT 13	THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD ALL CITATIONS AVAILABLE IN THE RE FORMAT				

L42 ANSWER 7 OF 23 HCAPLUS COPYRIGHT 2002 ACS  
AN 2001:758791 'HCAPLUS  
TI **Semiconductor device** and a method of manufacturing the  
same  
IN Masuda, Masachika; Wada, Tamaki; Nishizawa, Hirotaka; Kagaya, Koich  
Iro  
PA Japan  
SO U.S. Pat. Appl. Publ.  
CODEN: USXXCO  
DT Patent  
LA English  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001031513	A1	20011018	US 2001-826965	20010406
PRAI	JP 2000-114352	A	20000414		

AB A **semiconductor device** comprising: a **resin**  
sealing body, plural **semiconductor chips** situated  
inside the **resin** sealing body and formed of **rectangular**  
-shaped plane surfaces, having a first main surface and second main  
surface facing each other, and having electrodes disposed on the first  
side of a first side and a second side of the first main surface, the  
first side and second side facing each other, and **leads** having  
inner parts situated inside the **resin** sealing body and outer  
parts situated outside the **resin** sealing body, the inner parts  
being electrically connected to the electrodes of the plural  
**semiconductor chips** via bonding wires, wherein: the  
first main surfaces are aligned in the same direction with their  
respective first sides situated on the same side, and the plural  
**semiconductor chips** are laminated in positions offset  
with respect to one another such that the electrodes of one of the  
mutually opposite **semiconductor chips** are situated  
further outside than the first sides of the other **semiconductor**  
**chips**.

08/28/2002 10/022,297

L42 ANSWER 8 OF 23 HCPLUS COPYRIGHT 2002 ACS  
AN 2001:404187 HCPLUS  
TI **Semiconductor device** manufacturing method, press die  
and guide rail including forming a crack perpendicular to an extension of  
the sealing **resin**  
IN Aoki, Hideji; Sekiya, Hidenori; Katou, Kenichirou; Nishitani, Hiromu  
PA Mitsubishi Denki Kabushiki Kaisha, Japan; Mitsubishi Electric Engineering  
Co., Ltd.  
SO U.S., 36 pp.  
CODEN: USXXAM  
DT Patent  
LA English  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6242287	B1	20010605	US 1998-44928	19980320
PRAI	JP 1997-270887	A	19971003		

AB Provided are a method for manufacturing a **semiconductor device** in which a sealing **resin** is prevented from being damaged and generation of a **resin** piece is suppressed, a press die for suppressing the generation of the **resin** piece, and a guide rail. A **frame** receiving die (11) includes a cavity (11d) having a **rectangular** contour shape seen on a plane which serves to house a sealing **resin** (3) therein, and a remaining gate housing section (11c) provided on any of four corners of the cavity (11d) corresponding to a remaining gate (3b) on a lower face of a corner (2a) of a **lead frame** (2). A lower gate punch (11a) is provided in a boundary portion between the cavity (11d) and the remaining gate housing section (11c). When the **lead frame** (2) is mounted on the **frame** receiving die (11), the sealing **resin** (3) is housed in the cavity (11d) and the remaining gate (3b) is housed in the remaining gate housing section (11c).  
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD  
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L42 ANSWER 9 OF 23 HCPLUS COPYRIGHT 2002 ACS  
 AN 2001:927930 HCPLUS

TI **Lead/read frame and semiconductor device.** [Machine Translation].

IN Takaike, Kazuo

PA Shinko Electric Industries Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 6 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001358275	A2	20011226	JP 2000-180858	20000616
AB	[Machine Translation of Descriptors]. The <b>semiconductor</b> component being the concave section where the loading aspect which the loading is done was formed to the base, with usual diaphragm processing squeezes the deep concave section, in the extent of being and the formation difficult the formation it is possible in the heat radiation board with processing, at the same time can prevent the exfoliation of the heat radiation board and the seal <b>resin</b> easily effectively is the <b>lead/read frame</b> is offered. <b>Semiconductor</b> component 12 of said heat radiation board 18 the loading aspect which the loading is done, squeezes the inner <b>lead/read</b> 24 which is connected electrically <b>semiconductor</b> component 12 of <b>rectangular</b> condition the <b>semiconductor</b> component 12 which the loading is done and by wire 32 and the like and 24 * * with in the <b>lead/read frame</b> 10 which is possessed in the heat radiation board 18 which the loading is done and heat radiation board 18, the formation is done in base 14 of concave section 16 of the <b>rectangular</b> condition which was formed by processing at the same time the bending part which the inner wall section of each angular section of concave section 16 the formation is done, pulls out and is dropped in penetration hole is formed 26 and 28.				

L42 ANSWER 10 OF 23 HCPLUS COPYRIGHT 2002 ACS  
AN 2001:760781 HCPLUS  
TI Production method of the substrate and the **semiconductor**  
device which uses this. [Machine Translation].  
IN Enzan, Takao; Sasaki, Atsuo; Nokita, Kanta; Ishihara, Masamichi  
PA Mitsui High-Tec, Inc., Japan  
SO Jpn. Kokai Tokkyo Koho, 8 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001291795	A2	20011019	JP 2000-106961	20000407

AB [Machine Translation of Descriptors]. In the **semiconductor**  
**device** of flip tip/**chip** type of **resin** seal  
type, not yet filling up of the seal **resin** at the time of  
**resin** seal and occurring of void are prevented. As has of  
**rectangular** base material 2 the **rectangular**  
**semiconductor chip** loading territory 3 all over, the  
specified wiring pattern which from **semiconductor chip**  
loading territory 3 is expanded in outside direction is done, the  
formation with the insulated layer the covering doing the whole surface  
which excludes the land 5 of the wiring pattern, the formation does in the  
gate territory with all of the **semiconductor chip**  
loading territory 3 which is connected 17 which becomes, the filler inlet  
of the seal **resin** of the insulated **layer** in the  
baseplate 1 A which becomes, and the gate territory as thin section 6 A,  
the formation does with the other parts as thick section 6 B.

L42 ANSWER 11 OF 23 HCPLUS COPYRIGHT 2002 ACS

AN 2001:727470 HCPLUS

TI Production method of **lead/read frame** and  
**semiconductor device**. [Machine Translation].

IN Yasunaga, Hisashi; Sugimoto, Atsushi

PA Mitsui High-Tec, Inc., Japan

SO Jpn. Kokai Tokkyo Koho, 7 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001274308	A2	20011005	JP 2000-82091	20000323

AB [Machine Translation of Descriptors]. As penetration of the **resin** to **lead/read** of back side is prevented, when cutting off in each **semiconductor device**, exfoliation of **lead/read** and the seal **resin** is prevented. Through tie bar 6, combines the unit **frame** 2 which and possesses the **lead/read** 2 r of the feature which surrounds tip/**chip** loading limits 2 B in each side of **rectangular** plane surface plural gathers and the unit **frame** aggregate guide rail 5 g and the guide rail 5 g which are provided furthermore to outside tesseral of notch 5 S and the notch 5 S which were formed to outside tesseral of peripheral tie bar 6 o and the peripheral tie bar 6 o where combines unit **frame** 2 to the peripheral section of 7 which is formed and unit **frame** aggregate 7 and the combined piece 5 r which combines with peripheral tie bar 6 o forms **lead/read** Doing form processing of **frame**, 5 unit **frame** aggregate including with the portion of 7 and guide rail and 5 g the lumping together doing excluding back **resin** seals forms, this the cutting separation it does tie bar 6 and alongside with peripheral tie bar 6 o.

L42 ANSWER 12 OF 23 HCPLUS COPYRIGHT 2002 ACS  
AN 2001:357365 HCPLUS  
TI **Lead/read frame and semiconductor**  
device and the production method. [Machine Translation].  
IN Yugawa, Masayuki  
PA Matsushita Electronics Corp., Japan  
SO Jpn. Kokai Tokkyo Koho, 7 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
	-----	-----	-----	-----	-----
PI	JP 2001135766	A2	20010518	JP 1999-313421	19991104

AB [Machine Translation of Descriptors]. The case where the **resin** seals the **lead/read frame** which the **semiconductor** component the loading is done occurrence of void is retarded. In the underside of the point of plural inner **leads** /reads 11, heat radiation board 12 through insulated **resin** **layer** 13, is kept, **semiconductor** component 14 is mounted in the central part of heat radiation board, 12 is connected the electrode by the wire 16 where the point of 15 which is provided on the **semiconductor** component and inner **lead/read** 11 consists of the gold and the like. And, penetration hole 17 of spindle condition or **rectanglular** condition is provided in the corner section of heat radiation board 12.

L42 ANSWER 13 OF 23 HCPLUS COPYRIGHT 2002 ACS  
AN 2001:281335 HCPLUS  
TI **Semiconductor** luminous device. [Machine Translation].  
IN Maekawa, Mamoru  
PA Rohm Co., Ltd., Japan  
SO Jpn. Kokai Tokkyo Koho, 5 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE	
	-----	-----	-----	-----	-----	
PI	JP 2001111115	A2	20010420	JP 1999-289606	19991012	
AB	[Machine Translation of Descriptors]. Offer the tip/ <b>chip</b> type luminous device which is made the constitution which improves the brightness of the direction which is parallel with mounted direction without receiving the condition to the automated implementation. <b>Semiconductor</b> luminous device 10, the baseplate is formed notch 7 X and 8 X on 2 which the formation is done and the baseplate on the both ends, electrode pattern for the abbreviation center section of 3 of the pair where one terminal 3 X and 4 X cover aforementioned notch, 4 and the baseplate surface the luminous die (LED) tip/ <b>chip</b> 1st translucent <b>resin</b> mold 6 A of the condition which seals 1 which the loading is done and the aforementioned LED tip/ <b>chip</b> and, has with the 2nd translucent <b>resin</b> mold 6 B of the <b>rectangular</b> condition which is arranged in the surrounding. As 1st index of refraction of the translucent <b>resin</b> is selected 2nd more largely than index of refraction of the translucent <b>resin</b> , extending resident in can point to the both ends section of 2nd translucent <b>resin</b> mold to the end of baseplate 2.					

L42 ANSWER 14 OF 23 HCPLUS COPYRIGHT 2002 ACS  
AN 2002:78366 HCPLUS  
DN 136:111355  
TI **Semiconductor device** to emit heat from a  
semiconductor chip to a mother board  
IN Lee, Seon Gu; Han, Im Taek  
PA Amkor Technology Korea, Inc., S. Korea  
SO Repub. Korean Kongkae Taeho Kongbo, No pp. given  
CODEN: KRXXA7  
DT Patent  
LA Korean  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE	
	-----	---	-----	-----	-----	
PI	KR 2000019224	A	20000406	KR 1998-37202	19980909	
AB	A <b>semiconductor device</b> is provided to emit heat from a semiconductor chip to a mother board and be capable of encapsulating by using a transfer molding. A <b>semiconductor</b> device comprises: a flat-board heat spreader having a rectangular spreader penetrating portion in the center; a printed circuit board (PCB) having a board penetrating portion connected with the spreader penetrating portion while the heat spreader adheres to the PCB by inserting an <b>adhesive</b> ; a sub-heat spreader elongated and adhered to a bottom surface of the board penetrating portion by thermal conductive solder; a <b>semiconductor chip</b> adhered to inside of the board penetrating portion of the PCB, the top surface of the sub-heat spreader; wire for connecting the <b>semiconductor chip</b> with the PCB; encapsulant filled up in the board penetrating portion of the PCB and the spreader penetrating portion of the heat spreader to protect the <b>semiconductor chip</b> and the wire from the exterior circumstances; and solder balls for having the mother board elec. communicate with the <b>semiconductor chip</b> while being adhered to the bottom surface of the PCB.					

08/28/2002 10/022,297

L42 ANSWER 15 OF 23 HCPLUS COPYRIGHT 2002 ACS  
AN 2000:769684 HCPLUS  
DN 133:343402  
TI Manufacture of **resin**-packaged **semiconductor**  
devices  
IN Sukekawa, Hirokazu; Yoshida, Isamu; Amano, Yasuo  
PA Hitachi Maxell, Ltd., Japan; Hitachi, Ltd.  
SO Jpn. Kokai Tokkyo Koho, 6 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000306935	A2	20001102	JP 1999-116715	19990423

AB Bump contacts are formed on resp. pads of **semiconductor**  
**devices**, **rectangular** plate-shaped **leads** are  
connected across the bump contacts for each pad, and the  
**semiconductor devices** and the base of **lead**  
terminals are molded by thermosetting **resins**.

08/28/2002 10/022,297

L42 ANSWER 16 OF 23 HCPLUS COPYRIGHT 2002 ACS  
AN 2000:741353 HCPLUS  
DN 133:303293  
TI **Semiconductor LED devices, semiconductor**  
photosensor **devices** and array  
IN Yanagase, Masashi; Konishi, Yasuhiro; Imamoto, Hiroshi; Takaoka, Motoaki;  
Yama, Yoshikazu  
PA Omron Corp., Japan  
SO Jpn. Kokai Tokkyo Koho, 22 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000294831	A2	20001020	JP 1999-101894	19990408
AB	The devices comprise: a glass substrate; a LED or a photosensor <b>chip</b> ; a <b>rectangular</b> silicon cavity coated with a Au (or Ag) reflector; a <b>resin</b> encapsulation on the LED <b>chip</b> ; and the array package on the LED's or the photosensors.				

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

L42 ANSWER 17 OF 23 HCAPLUS COPYRIGHT 2002 ACS  
AN 2000:687757 HCAPLUS  
TI **Semiconductor device**. [Machine Translation].  
IN Suzuki, Takeshi  
PA Toshiba Corp., Japan  
SO Jpn. Kokai Tokkyo Koho, 10 pp.  
CODEN: JKXXAF  
DT Patent  
LA Japanese  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000269395	A2	20000929	JP 1999-73062	19990318
AB	[Machine Translation of Descriptors]. Improving the heat dissipation, improves allowance loss, offers the <b>semiconductor device</b> which can prevent the thermal destruction of the component. Besides the fact that outside outside in mold was connected 2 of the <b>rectangular</b> condition which the <b>resin</b> seals the tip/ <b>chip</b> where <b>semiconductor</b> circuit was formed and aforementioned <b>semiconductor</b> circuit and was formed to the one side of outer circle of mold, 2 possesses specified <b>lead/read</b> width in <b>lead/read</b> terminal was connected 4 and <b>semiconductor</b> circuit and was formed to the aforementioned one side, possesses the <b>lead/read</b> width of 4 times that or more aforementioned specified <b>lead/read</b> width in <b>lead/read</b> terminal is connected 6 and <b>semiconductor</b> circuit and opposes to the aforementioned one side outside was formed to the side, possesses the <b>lead/read</b> width of 4 times that or more aforementioned specified <b>lead/read</b> width has possessed with <b>lead/read</b> terminal 8.				

L42 ANSWER 18 OF 23 HCPLUS COPYRIGHT 2002 ACS

AN 2000:666433 HCPLUS

TI Surface mounted type **semiconductor device**. [Machine Translation].

IN Ootomo, Masahiro; Tsuboi, Yoshiji

PA Toshiba Corp., Japan

SO Jpn. Kokai Tokkyo Koho, 4 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
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PI JP 2000260926 A2 20000922 JP 1999-63052 19990310

AB [Machine Translation of Descriptors]. The **resin** being lacking around the support bar is prevented, the mounted type **semiconductor device** which does not have the mounted error to the baseplate is offered. **Semiconductor chip** 4 adheres in order the die padding for back of 3 where and this die padding 3 to expose in appearance, as the aforementioned **semiconductor chip** is molded, the underside almost forms the **rectangular** mounted aspect the plastic package 2 where and the one terminal in inside aforementioned plastic package 2, is connected by aforementioned **semiconductor chip** 4, in order for other edge to expose in the side of aforementioned package mounted aspect 8, as is bent in the aforementioned package underside vicinity connection **lead/read** 10 outside and the one terminal is bonded to aforementioned die padding 3, other edge to corner section 9 of aforementioned package mounted aspect 8 In order to expose, has with the support bar 15 which is bent inside the aforementioned package, as for aforementioned exposure end 16 of this support bar, in order to occupy the corner section 9 of aforementioned package mounted aspect 8 substantially, the area is expanded.

L42 ANSWER 19 OF 23 HCAPLUS COPYRIGHT 2002 ACS  
 AN 2000:88745 HCAPLUS  
 TI **Semiconductor device**. [Machine Translation].  
 IN Suzuki, Nobuaki; Sano, Masashi; Suzuki, Shinichi  
 PA Rohm Co., Ltd., Japan  
 SO Jpn. Kokai Tokkyo Koho, 17 pp.  
 CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000040781	A2	20000208	JP 1998-246023	19980831
	EP 1089335	A1	20010404	EP 1999-918314	19990430
	R: DE, GB, NL				
	TW 413834	B	20001201	TW 1999-88108022 19990518	

PRAI JP 1998-138691 A 19980520  
 JP 1998-138692 A 19980520  
 JP 1998-246023 A 19980831  
 WO 1999-JP2357 W 19990430

AB [Machine Translation of Descriptors]. Degree of freedom of choice of mounting direction of the **semiconductor device** in the case where the **semiconductor device** is mounted on the circuit baseplate and the like is raised. As in the **resin** package 4 which, was formed to the form of the plane surface apparent abbreviation **rectangular** condition which possesses specified thickness **lead/read lead/read 20** inside 10 inside 1st the formation is done and 2nd and, continues in **lead/read 10** inside 1st as outside **resin** package 4 **lead/read 11** outside 1st the formation is done and, continues in **lead/read 20** inside 2nd, **lead/read 21** outside 2nd was formed outside **resin** package 4 and, in the **semiconductor device** X which has, **lead/read lead/read 21** outside 11 outside 1st and 2nd, those basic ends 11 A 21 A that tried parallels to the side 41 of **resin** package 4 (42), from each basic end 11 A and 21 A furthermore **lead/read 11** each outside continues, 21 to parallel to the base 45 of **resin** package 4 tried.

L42 ANSWER 20 OF 23 HCPLUS COPYRIGHT 2002 ACS  
AN 2000:203176 HCPLUS  
TI Light radiating **semiconductor device** with a reflector  
[Machine Translation].  
IN Ishinaga, Hiroki  
PA Rohm Co. Ltd., Japan  
SO Ger. Offen.  
CODEN: GWXXBX  
DT Patent  
LA German  
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19945919	A1	20000330	DE 1999-19945919	19990924
	JP 2000101149	A2	20000407	JP 1998-270790	19980925
PRAI	JP 1998-270790		19980925		

AB [Machine Translation of Descriptors]. A light radiating **semiconductor device** contains a substrate 12. This substrate is formed with a pair electrode courses 14, 16 on it. One of the electrode courses has a **rectangular** line range, on which a light radiating **semiconductor chip** 25 is form-connected. That light radiating **semiconductor chip** is strength-connected on the other side with the other electrode course. A reflector is formed for spritz-Formen of a liquid crystalline **polymer** on the substrate over. The reflector has a passage cutout, which is formed at its central range, and which exhibits an internal surface, which is coated with a metal. That light radiating **semiconductor chip** is arranged, and a translucent **epoxy resin** 36 with a glass transition temperature of 60.degree.C or among them into the passage cutout is filled within the passage cutout, in order to form thereby a shroud body.

L42 ANSWER 21 OF 23 HCPLUS COPYRIGHT 2002 ACS  
AN 1999:756885 HCPLUS  
DN 131:359164  
TI **Semiconductor devices** for photosensor component  
packages  
IN Sano, Masashi; Suzuki, Nobuaki; Suzuki, Shinichi  
PA Rohm Co., Ltd., Japan  
SO Jpn. Kokai Tokkyo Koho, 14 pp.  
CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11330131	A2	19991130	JP 1998-138692	19980520
	EP 1089335	A1	20010404	EP 1999-918314	19990430

R: DE, GB, NL

TW 413834 B 20001201

PRAI	JP 1998-138691	A	19980520		
	JP 1998-138692	A	19980520		
	JP 1998-246023	A	19980831		
	WO 1999-JP2357	W	19990430		

AB The title devices comprise a wide 1st inner **lead** wire having a **chip**-mounting dia-bonding region, a 2nd **lead** wire having a wire-bonding region connected via a **semiconductor chip** and a wire, a **rectangular** plastic package with a desired width for packaging in with a **semiconductor chip** or the 2nd inner **lead** wire, and a 1st outer **lead** wire connected to the 1st inner **lead** wire and formed on the outside the package. The die-bonding region is provided at a position shifted from the center of the package and the wire-bonding region is provided at the center or its proximity. The arrangement of the bonding regions avoids breaking of the wires in the package.

08/28/2002 10/022,297

L42 ANSWER 22 OF 23 HCPLUS COPYRIGHT 2002 ACS

AN 1994:568436 HCPLUS

DN 121:168436

TI Opening window on **resin film** on **semiconductor device**

IN Kajiwara, Satomi

PA Fuji Electric Co Ltd, Japan

SO Jpn. Kokai Tokkyo Koho, 5 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06140317	A2	19940520	JP 1992-284797	19921023
	JP 3151964	B2	20010403		

AB In opening a **rectangular** window on semicured **coated resin film** on a **chip**-installed wafer by liq. etchant, the corners of the window-corresponding pattern of a photoresist etching mask is round off to make the radius of curvarture .gtoreq.1.5 times than the **film** thickness of the **resin film**. The **resin** may be **polyimide**, the window may be opened simultaneously with treatment of the photoresist by a developer as an etchant, and the photoresist may be dissolved out by a solvent after opening the window.

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L42 ANSWER 23 OF 23 HCPLUS COPYRIGHT 2002 ACS

AN 1994:287375 HCPLUS

DN 120:287375

TI **Resin-potted semiconductor device**

IN Okuaki, Yutaka

PA Oki Electric Ind Co Ltd, Japan

SO Jpn. Kokai Tokkyo Koho, 4 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 05259362	A2	19931008	JP 1992-51976	19920311

AB The title device employs a **lead frame** comprising a **rectangular** tab for mounting a **semiconductor chip**, nobs protruding through the potting **resin** along the long sides of the tab; and H2O-repellent coating film formed on at least 1 side of each tab.